Refine Search

Search Results -

Term	Documents
(2 AND 8).PGPB,USPT.	23
(L2 AND L8).PGPB,USPT.	23

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L17

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Tuesday, May 24, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT; PLUR=YES; OP=OR			
L17	l2 and l8	23	L17
L16	l2 and l7	9	L16
L15	l2 and l6	8	L15
L14	l2 and l4	85	L14
L13	l3 and L8	6	L13
L12	l3 and L7	3	L12
L11	l3 and L6	8	L11
L10	l3 and L5	34	L10
L9	l3 and L4	34	L9
L8	(711/147-221)[CCLS]	15789	L8
L7	(712/225, 229)[CCLS]	497	L7
L6	(712/24)[CCLS]	246	L6
L5	(712/2-300)![CCLS]	10993	L5

L4	(712/2-300)[CCLS]	10993	L4
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2 and (vliw$1 or very near1 large)	44	L3
L2	L1 near8 (designat$4 or specif$5)	164	L2
L1	(select$5 or multiplex$5) near6 register near1 files	2156	L1

END OF SEARCH HISTORY

Results for "((register <near/5> file* <and> (select*, multiplex*, mux))<in>metadata)" e-mail

Your search matched **31** of **1164322** documents.

A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» View Session History

» New Search

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

((register <near/5> file* <and> (select*, multiplex*, mux))<in>metadata)

Check to search only within this results set

Display Format: Citation Citation & Abstract

Select Article Information

1. **Synthesis of Signal Processing Structured Datapaths for FPGAs Supporting RAMs and Busses**
Haroun, B.; Sajjadi, B.;
Field-Programmable Gate Arrays, 1995. FPGA '95. Proceedings of the Third International ACM Symposium c
1995 Page(s):75 - 81
AbstractPlus | Full Text: PDF(160 KB) IEEE CNF

2. **A 150-MOPS GaAs 8-bit slice processor**
Gauthier, R.V.; Weissman, J.; Peterson, B.E.; Florez, J.M.;
Solid-State Circuits, IEEE Journal of
Volume 23, Issue 5, Oct. 1988 Page(s):1195 - 1202
AbstractPlus | Full Text: PDF(612 KB) IEEE JNL

3. **An efficient technique for exploring register file size in ASIP design**
Jain, M.K.; Balakrishnan, M.; Kumar, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 23, Issue 12, Dec. 2004 Page(s):1693 - 1699
AbstractPlus | References | Full Text: PDF(304 KB) IEEE JNL

4. **A 130-nm 6-GHz 256 × 32 bit leakage-tolerant register file**
Krishnamurthy, R.K.; Alvandpour, A.; Balamurugan, G.; Shanbhag, N.R.; Soumyanath, K.; Borkar, S.Y.;
Solid-State Circuits, IEEE Journal of
Volume 37, Issue 5, May 2002 Page(s):624 - 632
AbstractPlus | References | Full Text: PDF(319 KB) IEEE JNL

5. **Analysis of the influence of register file size on energy consumption, code size, and execution time**
Wehmeyer, L.; Jain, M.K.; Steinke, S.; Marwedel, P.; Balakrishnan, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 20, Issue 11, Nov. 2001 Page(s):1329 - 1337
AbstractPlus | References | Full Text: PDF(320 KB) IEEE JNL

6. **A 2-GHz clocked AlGaAs/GaAs HBT byte-slice datapath chip**
Carlough, S.R.; Philhower, R.A.; Maier, C.A.; Steidl, S.A.; Campbell, P.M.; Garg, A.; Kyung-Suc Nah; Ernest, Krawczyk, T.W., Jr.; Curran, P.F.; Kraft, R.P.; Greub, H.J.; McDonald, J.F.;
Solid-State Circuits, IEEE Journal of
Volume 35, Issue 6, June 2000 Page(s):885 - 894
AbstractPlus | References | Full Text: PDF(748 KB) IEEE JNL

7. **A 500-MHz, 32-word×64-bit, eight-port self-resetting CMOS register file**
Wei Hwang; Joshi, R.V.; Henkels, W.H.;
Solid-State Circuits, IEEE Journal of
Volume 34, Issue 1, Jan. 1999 Page(s):56 - 67
AbstractPlus | References | Full Text: PDF(412 KB) IEEE JNL

8. **Nonscan design-for-testability techniques using RT-level design information**
Dey, S.; Potkonjak, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 16, Issue 12, Dec. 1997 Page(s):1488 - 1506
AbstractPlus | References | Full Text: PDF(340 KB) IEEE JNL

9. **Datapath synthesis using onchip multiport memories**
Ahmad, I.; Chen, C.Y.R.;
Computers and Digital Techniques, IEE Proceedings-
Volume 140, Issue 4, Jul 1993 Page(s):227 - 232
AbstractPlus | Full Text: PDF(388 KB) IEE JNL

10. **The energy complexity of register files**
Zyuban, V.; Kogge, P.;
Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on
10-12 Aug 1998 Page(s):305 - 310
AbstractPlus | Full Text: PDF(688 KB) IEEE CNF

11. **A GaAs 32-bit RISC microprocessor**
Harrington, D.L.; Troeger, G.L.; Gee, W.C.; Bolen, J.A.; Vogelsang, C.H.; Nicalek, T.P.; Lowe, C.M.; Roh, Y.K
J.F.; Reeder, J.;
Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1988. Technical Digest 1988., 10th Annual IEEE
6-9 Nov. 1988 Page(s):87 - 90
AbstractPlus | Full Text: PDF(248 KB) IEEE CNF

12. **Interconnect optimisation during data path allocation**
Stok, L.;
Design Automation Conference, 1990. EDAC. Proceedings of the European
12-15 March 1990 Page(s):141 - 145
AbstractPlus | Full Text: PDF(396 KB) IEEE CNF

13. **A heuristic for data path synthesis using multiport memories**
Ahmad, I.; Chen, C.Y.R.;
VLSI, 1992., Proceedings of the Second Great Lakes Symposium on
28-29 Feb. 1992 Page(s):44 - 51
AbstractPlus | Full Text: PDF(564 KB) IEEE CNF

14. **An environment for evaluating architectures for spatially mapped computation: System architecture a**
Herbordt, M.C.; Weems, C.C.;
Computer Architectures for Machine Perception, 1993. Proceedings
15-17 Dec. 1993 Page(s):191 - 201
AbstractPlus | Full Text: PDF(760 KB) IEEE CNF

15. **Synthesis of memories from behavioral HDLs**
Vander Zanden, N.;
ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International
19-23 Sept. 1994 Page(s):71 - 74
AbstractPlus | Full Text: PDF(260 KB) IEEE CNF

16. **Multithreaded vector architectures**

Espasa, R.; Valero, M.;
High-Performance Computer Architecture, 1997., Third International Symposium on
1-5 Feb. 1997 Page(s):237 - 248

AbstractPlus | Full Text: PDF(1248 KB) IEEE CNF

17. **A graph-theoretic approach for register file based synthesis**
Ravikumar, C.P.; Aggarwal, R.; Sharma, C.;
VLSI Design, 1997. Proceedings., Tenth International Conference on
4-7 Jan. 1997 Page(s):118 - 123

AbstractPlus | Full Text: PDF(500 KB) IEEE CNF

18. **An eight-issue tree-VLIW processor for dynamic binary translation**
Ebcioglu, K.; Fritts, J.; Kosonocky, S.; Gschwind, M.; Altman, E.; Kailas, K.; Bright, T.;
Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., International Conferen
5-7 Oct. 1998 Page(s):488 - 495

AbstractPlus | Full Text: PDF(108 KB) IEEE CNF

19. **Teaching computer architecture/organisation using simulators**
Grunbacher, H.;
Frontiers in Education Conference, 1998. FIE '98. 28th Annual
Volume 3, 4-7 Nov. 1998 Page(s):1107 - 1112 vol.3

AbstractPlus | Full Text: PDF(1664 KB) IEEE CNF

20. **A 690 ps read-access latency register file for a GHz integer microprocessor**
Takahashi, O.; Silberman, J.; Dhong, S.; Hofstee, P.; Aoki, N.;
Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., International Conferen
5-7 Oct. 1998 Page(s):6 - 10

AbstractPlus | Full Text: PDF(820 KB) IEEE CNF

21. **Automated design of wave pipelined multiport register files**
Takano, K.; Sasaki, T.; Oba, N.; Kobayashi, H.; Nakamura, T.;
Design Automation Conference 1998. Proceedings of the ASP-DAC '98. Asia and South Pacific
10-13 Feb. 1998 Page(s):197 - 202

AbstractPlus | Full Text: PDF(548 KB) IEEE CNF

22. **Memory design and exploration for low power, embedded systems**
Wen-Tsong Shiue; Chakrabarti, C.;
Signal Processing Systems, 1999. SiPS 99. 1999 IEEE Workshop on
20-22 Oct. 1999 Page(s):281 - 290

AbstractPlus | Full Text: PDF(508 KB) IEEE CNF

23. **A 0.29 ns 32-word by 32 b three-port bipolar register file implemented using a SiGe HBT BiCMOS tech**
Steidl, S.A.; McDonald, J.F.;
Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE International
15-17 Feb. 1999 Page(s):194 - 195

AbstractPlus | Full Text: PDF(236 KB) IEEE CNF

24. **Determining the optimum extended instruction-set architecture for application specific reconfigurable**
Alippi, C.; Fornaciari, W.; Pozzi, L.; Sami, M.;
Rapid System Prototyping, 12th International Workshop on, 2001.
25-27 June 2001 Page(s):50 - 56

AbstractPlus | Full Text: PDF(596 KB) IEEE CNF

25. **Exploiting loop-level parallelism with the Shift Architecture**
Lima, C.D.; Nakamura, T.;
Computer Architecture and High Performance Computing, 2002. Proceedings. 14th Symposium on
28-30 Oct. 2002 Page(s):184 - 191

AbstractPlus | Full Text: PDF(298 KB) IEEE CNF

Results for "((register <near/5> file* <and> (select*, multiplex*, mux))<in>metadata)".
Your search matched **31** of **1164322** documents.
A maximum of **31** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» View Session History

» New Search

Modify Search

((register <near/5> file* <and> (select*, multiplex*, mux))<in>metadata)

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

26. **Register write specialization register read specialization: a path to complexity-effective wide-issue su**
Seznec, A.; Toullec, E.; Rochecouste, O.;
Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on
18-22 Nov. 2002 Page(s):383 - 394
AbstractPlus | Full Text: PDF(294 KB) IEEE CNF

27. **A 90 nm 6.5 GHz 256/spl times/64 b dual supply register file with split decoder scheme**
Hsu, S.; Chatterjee, B.; Sachdev, M.; Alvandpour, A.; Krishnamurthy, R.K.; Borkar, S.;
VLSI Circuits, 2003. Digest of Technical Papers. 2003 Symposium on
12-14 June 2003 Page(s):237 - 238
AbstractPlus | Full Text: PDF(295 KB) IEEE CNF

28. **Hierarchical clustered register file organization for VLIW processors**
Zalamea, J.; Llosa, J.; Ayguade, E.; Valero, M.;
Parallel and Distributed Processing Symposium, 2003. Proceedings. International
22-26 April 2003 Page(s):10 pp.
AbstractPlus | Full Text: PDF(391 KB) IEEE CNF

29. **Register aware scheduling for distributed cache clustered architecture**
Zhong Wang; Xiaobo Sharon Hu; Sha, E.H.-M.;
Design Automation Conference, 2003. Proceedings of the ASP-DAC 2003. Asia and South Pacific
21-24 Jan. 2003 Page(s):71 - 76
AbstractPlus | Full Text: PDF(764 KB) IEEE CNF

30. **A 64-state 2GHz 500Mbps 40mW Viterbi accelerator in 90nm CMOS**
Anders, M.; Mathew, S.; Krishnamurthy, R.; Borkar, S.;
VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on
17-19 June 2004 Page(s):174 - 175
AbstractPlus | Full Text: PDF(288 KB) IEEE CNF

31. **Performance analysis of inter cluster communication methods in VLIW architecture**
Saluja, S.; Kumar, A.;
VLSI Design, 2004. Proceedings. 17th International Conference on
2004 Page(s):761 - 764
AbstractPlus | Full Text: PDF(254 KB) IEEE CNF